WHAT IS CLAIMED IS:

1. A method of time tracking in a vector correlator, comprising the steps of:

(a) providing a vector correlator based system having a triple data input buffer having three parts wherein two of the three parts are available for processing by a correlator datapath while the remaining part is being written into by incoming chips, and further wherein one of the two parts of the triple data input buffer available for processing contains a plurality of early sets of chips while the remaining part contains a plurality of temporally late sets of chips;

(b) receiving chip samples into the triple data input buffer; and

(c) despreading a plurality of triple data input buffer chips selected from the two buffers available for processing by the correlator datapath in a single correlation processing cycle.

2. The method according to claim 1 further comprising the steps of:

(d) detecting a timing change associated with the chip samples via commands transmitted to the vector correlator from a host processor;

(e) detecting an event where a timing change to an earlier chip sample is commanded by the host processor while the current chips being processed are the earliest in the triple data input buffer, and the sample being processed is the earliest sample;

(f) depreading the latest samples of chips from the latest third within the triple data input buffer upon completion of the timing change command by the host processor; and

(g) depreading via parallel processing the earliest third of the triple data input buffer chips in the same correlation processing cycle as the latest third of the triple data input buffer chips.

3. The method according to claim 1 further comprising the steps of:

(d) detecting an event where a timing change to a later sample is commanded by the host processor while the current chips being processed are the latest in the triple data input buffer, and the sample being processed is the latest sample;

skipping one correlation cycle upon the occurrence of the event; and

despreading the earliest sample of each chip associated with the earliest set of chips in the triple data input buffer upon completion of the timing change command by the host processor and subsequent to the skipped correlation cycle.

4. A method of time tracking in a vector correlator, comprising the steps of:

(a) providing a vector correlator based Rake receiver having a triple data input buffer having two parts available for processing by a correlator datapath while a remaining part is being written into by incoming chips, wherein one of the two parts available for processing by the correlator datapath contains a plurality of early sets of chips while the remaining part contains a plurality of temporally late sets of chips;

(b) receiving chip samples into the triple data input buffer;

(c) detecting early, ontime and late timing changes associated with the received chip samples via commands transmitted to the vector correlator from a host processor;

(d) despreading in a single processing cycle, a plurality of triple data input buffer chips selected from the two buffers available for processing by the correlator datapath;

(e) despreading the plurality of the earliest third of the triple data input buffer chips and the plurality of latest third of the triple data input buffer chips in a single correlation processing cycle subsequent to wrapping the earliest set of chip samples back into the latest input buffer portion such that latest input buffer chips can be processed in response to the timing change to implement time tracking in subsequent processing cycles; and

(f) skipping one correlation processing cycle when the latest input buffer chips are to be processed and the timing change indicates time tracking need to be done to a later chip sample that falls outside the latest third of the triple data input buffer chip portion.

5. The method according to claim 4 further comprising the steps of:

(g) despreading the plurality of the earliest third of the triple data input buffer chips and the plurality of latest third of the triple data input buffer chips in a single correlation processing cycle subsequent to wrapping the earliest set of chip samples back into the latest input buffer portion such that latest input buffer chips can be processed in response to the timing change to implement time tracking in subsequent processing cycles.

6. The method according to claim 4 further comprising the steps of:

(g) skipping one correlation processing cycle when the latest chips in the triple data input buffer are being processed and the timing change indicates time tracking needs to be done to a later chip sample that falls outside the input buffer; and

(h) despreading the plurality of earliest chips in the input buffer in response to the timing change and subsequent to the skipped correlation processing cycle.